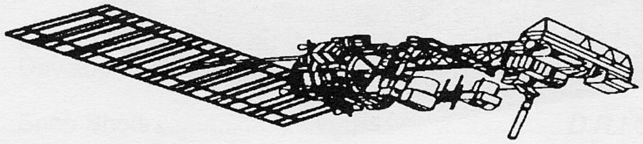
May 1992 Number 5

Weather Satellite Report



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Technical Feature

A PRBS Split Phase Generator

Whether you just completed your bit-synchronizer kit or even made a design of your own, now comes the time to test it. Lucky you, if all other parts of your HRPT system are already up and running, since under these circumstances you may perform the test under real world conditions. This generator is for the rest of us, who build their system from scratch.

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PRBS stands for "pseudo random binary sequence" and before we discuss the circuit details we will show how testing with this generator is implemented. Assume an nrz sequence of binary information with a bit rate equal to that of the intended satellite. Since the signal is transmitted in bi-phase-l or split-phase we do not get the bit sequence itself from the receiver's demodulated output. Instead we get the bi-phase representation of the original sequence. Now assume a circuit that not only produces a certain bit sequence, but also the bi-phase representation of this bit sequence.

Next, feed the bi-phase output of the circuit into the demodulator input of the bit-synchronizer. The synchronizer's job is to decode the bi-phase data into the original nrz bit sequence. Since we have the original bit sequence at hand by means of the generating circuit, we can compare the generated bit sequence to that pouring out of the synchronizer: If they are the same (or perhaps delayed by one clock cycle), the synchronizer is okay.

Comparing one bit to another can be a difficult task if they change with a few 100000 kHz! Therefore we have to use a bit sequence with certain properties: Some degree of random to make it look as a real world signal but also some kind of "repeatability" to make it predictive. That is exactly what the described circuit does. It is based loosely on ideas presented in *A METEOSAT Primary Data User Station,* from The University of Dundee.

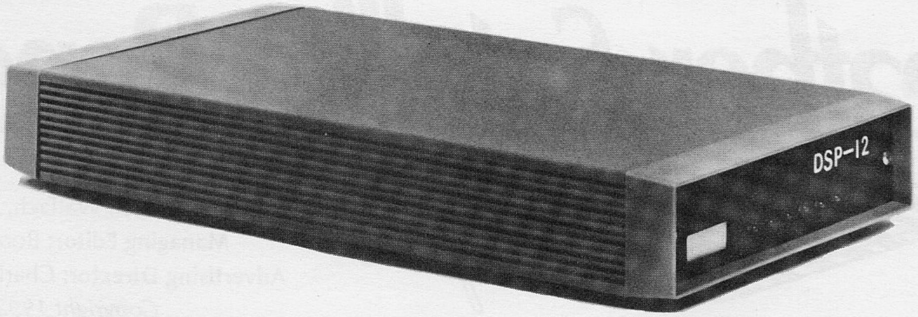
While the original circuit worked only for a bit rate of 166.66 kHz (as used with METEOSAT) and was based on a hard-to-get 166.66 kHz crystal, we choose to make it work with an inexpensive integrated 4 MHz oscillator and to cover METEOSAT as well as GOES bit rates. Notice that the circuit does not exactly produce the 665.4 kHz bit rate of the GOES birds, but 666.66 kHz, which is only 0.18 % apart should lead to no difficulties as long as your synchronizer is based on a PLL with a real VCO. Care should be taken if your synchronizer

(Continued on page 3)

On a Different Subject:

This setup was put together by Charlie Davis, Sr. See details on page 4.

VERSATILITY PLUS +



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In This Issue...

Index to Advertisers

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works with a VCXO since the capture range of the crystal-based circuits might not be great enough to lock on the generator's signal.

U8, in the circuit diagram, produces the 4 MHz clock signal. The first two stages of counter U5a together with U4c form a divider by three. The third stage of U5a divides by two, so we get a 4 MHz / 6 = 666.66 kHz clock at QC of U5a. This clock can be used to drive the rest of the circuit via a Jumper 1-2 of JP1. If we want to use the generator for METEOSAT emulation we again divide this clock by 4 (stage 4 of U5a and stage 1 of U5b) and use position 3-4 of JP1.

The main block of the circuit is the pseudo-random-generator consisting of U1, U2, U3a and U4a. It produces a random sequence of 2047 bits. Any kind of random generator based on shift register feedback from some stages to its input has a single "not allowed" state, since, being in that state, it produces no random bits anymore but reproduces the "not allowed" state. The not allowed state is a "0" in all stages of the shift register if we use normal feedback (that means: without inverting the feedback) and a "1" in all stages if we use inverted feedback. Since the 74HCT164 can safely be reset on power-up by means of C1 and R1 to a all-zero state, we need to use inverted feedback and therefore use inverter U3a.

Since the sequence is 2047 bits (and not 2048) long we cannot derive a trigger signal that is phase-stable relative to the sequence by simply dividing the clock by any integer. Instead, a different technique is used: Counter U6a has the same clock source as the shift register. The counter is reset to "0" whenever a "1" appears at stage 1 of the shift register, so it effectively counts the number of "0"s that wander through the register one after another. If 11 "0"s have wandered through stage 1 of the register (what happens exactly once per sequence with 11 stages of the register in use), a decimal "11" appears at the counter outputs. This condition is detected by U3b and U7 and signalized as "SEQUENCE REPEAT".

"SEQUENCE REPEAT", when used as a trigger signal for your scope, lets you see a stable picture of the sequence when monitoring "NRZ L DATA". It is a negative going pulse of clock-period / 2 duration. You might use one of the free inverters of U3 to make it a positive pulse. U4b produces a inverted split-phase signal. R2 and C2 remove glitches that have been introduced by propagation delays of the shift register and U3c converts the inverted split-phase to normal. The proposed values for R2 and C2 were chosen for the METEOSAT bit rate and are subject to be changed (smaller values) for GOES bit rates.

For the test, you need a dual channel scope with external trigger capability and a delayed time base. Connect "SEQUENCE REPEAT" to the scope's trigger input and "NRZ L DATA" to channel 1. Adjust trigger level and sweep time until you get a stable picture of a few bits of the sequence. Now connect "BI-PHASE DATA" to the synchronizer's input and the synchronizer's output to channel 2 of the scope. Switch scope to dual channel display.

If you see two identical traces in terms of transitions, your bit synchronizer is running perfectly. Please notice that according to the circuitry of the synchronizer, it's output (channel 2) may be delayed one clock cycle relative to the original signal (channel 1). This is perfectly okay since it has no influence on the further digital processing. Use the variable sweep delay of your scope to see other parts of the sequence. Remember that your scope is triggered only once per sequence so, if you make the scope display, say three bits of the se-

Split Phase Generator (from page 3)

quence, the trace writing speed is by a factor 2047 / 3 higher than the repetition rate resulting in a low intensity of the trace. So you might be forced to set a high intensity level at your scope to see anything at all. For this reason using an analog or digital storage scope is preferred.

In addition to comparing the data streams, you are free to compare "PHASE 0 CLOCK" to the clock output of the synchronizer. Please note that the described circuit is intended for tests on bit synchronizers exclusively. For tests that include word (frame) synchronizers one would need much more complex circuits that are capable of generating longer bit sequences which contain the sync words.

It is impractical to use PRBS sequences for that purpose because if the sequence is made long enough to contain the sync words the repetition rate of the sync information would be very low. ▌▌

Feature Weather Satellite Setup

The photographs on page 1, here, and on page 13 show the set up put together by Charlie Davis, Sr., column editor and Director of Advertising for *Weather Satellite Report.* Charlie describes the equipment below:

The oscilloscope from Ramsey Electronics is used for signal monitoring of all spacecraft transmitting on 137 MHz. The larger box next to the oscilloscope is a Wavetek SSI 3000B service monitor. This devised is used to watch the 137 MHz band for unknown signals, and to check the operating frequency of all the spacecraft monitored at this ground station. The service monitor is the most important piece of test equipment used here for satellite work. The two receivers are from Vanguard, one is a WEPIX 3000 and the other is a FMR-250-PL. Both are used for APT. The computer on the left is an

(Continued on page 13)